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VNA-based Insertion Loss and Return Loss Testing and De-embedding Techniques for High-Speed Serial Links on PCBs

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Abstract: This paper addresses the critical requirements of high-speed communication systems within artificial intelligence (AI) data centers, focusing on both theoretical analysis and practical implementation. The study begins with a detailed examination of the Vector Network Analyzer (VNA) measurement principle and the definition of S-parameters, providing an in-depth explanation of the physical significance of key parameters, including S11 and S21. The relationship between insertion loss and return loss is explored, highlighting their influence on signal fidelity and overall system performance. Furthermore, the characteristics of high-speed serial links are analyzed in conjunction with Pulse Amplitude Modulation 4-level (PAM4) signaling, emphasizing the effects of test indicators such as channel insertion loss flatness, group delay, and return loss margin on signal integrity. The paper also elaborates on the design and construction of the test system, including the deployment of de-embedding techniques to isolate and accurately measure channel effects. Experimental verification is conducted to assess system performance, with results analyzed to demonstrate the practical impact of different signal impairments on high-speed data transmission. Insights derived from the study provide valuable guidance for engineers and researchers involved in the design, testing, and optimization of high-speed interconnects in AI-driven data centers, offering concrete recommendations for improving signal reliability and overall communication efficiency.

Keywords: Vector Network Analyzer; PCB; high-speed serial link; insertion loss; return loss; de-embedding technology

1. Analysis of VNA Measurement Principles and High-Speed Serial Link Testing Requirements

1.1. High-Speed Serial Link Characteristics and Test Requirements

High-speed serial links are essential for high-bandwidth data transmission in artificial intelligence (AI) data centers, serving as the backbone for interconnects such as high-speed Ethernet and PCIe Gen5/6 interfaces. These links are designed to handle extremely high data rates while maintaining signal integrity across complex printed circuit board (PCB) layouts and connector interfaces. Pulse Amplitude Modulation 4-level (PAM4) technology is widely adopted in such environments due to its ability to double the data rate compared to traditional non-return-to-zero (NRZ) signaling. However, the use of PAM4 increases sensitivity to signal impairments, making precise testing and analysis critical.

Key test parameters for high-speed serial links include channel insertion loss flatness, group delay, and return loss margin. Channel insertion loss flatness reflects the uniformity of signal attenuation across the frequency band; deviations can result in amplitude distortion, inter-symbol interference, and reduced eye diagram opening. Group delay represents the variation in signal propagation time for different frequency components, directly impacting timing alignment and signal jitter. Return loss margin

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quantifies the proportion of signal energy reflected back due to impedance mismatches, ensuring that reflections remain within acceptable limits to prevent signal degradation and potential bit errors. Collectively, these parameters define the signal integrity landscape and guide engineers in optimizing high-speed link performance, including channel design, equalization strategies, and connector selection [1].

1.2. Test System Composition and Sources of Error

A typical VNA-based test system consists of a VNA host, test fixtures, probes, connectors, high-frequency cables, and calibration standards. In high-speed data center PCB testing, each component contributes to measurement uncertainty, potentially compromising the accuracy of S-parameter characterization. Parasitic elements, such as the inductance and capacitance of probes and fixtures, can cause impedance mismatches and increase return loss, while reflections and losses from connectors and cables introduce additional insertion loss errors. Calibration components, including precision loads, shorts, and opens, directly affect the system's ability to correct these errors, with their accuracy determining the effectiveness of the calibration process [2].

The VNA employs a comprehensive 12-term error model encompassing directivity, source and load match, reflection tracking, transmission tracking, crosstalk, and other higher-order terms. Calibration routines systematically eliminate these error contributions, enabling precise measurement of the true device under test (DUT) characteristics. Environmental conditions further complicate testing: temperature fluctuations can alter the dielectric properties of PCB materials, causing drift in measured S-parameters, while poor grounding can introduce common-mode noise, degrading measurement reliability. Accurate characterization of these factors is essential for high-speed link validation, as they influence both design verification and the optimization of system-level signal integrity strategies.

Beyond static measurements, understanding the dynamic behavior of high-speed links under operational conditions is increasingly important. Factors such as voltage supply fluctuations, simultaneous switching noise (SSN), and electromagnetic interference (EMI) can exacerbate signal degradation, highlighting the necessity for comprehensive testing that combines VNA measurements with time-domain reflectometry and bit-error-rate analysis. By integrating these approaches, engineers can achieve a holistic assessment of high-speed serial link performance, ensuring robust communication in AI data center applications [3].

2. Design of a VNA-Based Insertion Loss and Return Loss Testing System

2.1. Test System Architecture and Equipment Selection

The design of a VNA-based test system for insertion loss and return loss measurement requires careful consideration of the link's operating frequency, interface type, and PCB layout complexity. The selection of the VNA should ensure sufficient frequency range coverage to fully characterize the high-speed link. For example, a four-port VNA such as the Keysight N5247B, capable of operating up to 67 GHz, provides adequate bandwidth for differential measurements and supports comprehensive S-parameter acquisition.

The PCB sample must simulate realistic operational conditions, including representative channel lengths, differential pair routing, and high-density component placement. Differential pair design helps suppress common-mode noise and electromagnetic interference, which are critical factors in AI data center environments. The test fixture design employs GSSG (ground-signal-signal-ground) probes to maintain consistent grounding and minimize crosstalk, while SMA interfaces offer reliable, low-reflection connections. In high-density PCB layouts, the fixture's electromagnetic shielding performance is crucial to prevent external interference from affecting measurement accuracy. Additional considerations include minimizing trace

discontinuities, controlling impedance mismatches, and selecting low-loss materials for connectors and cables to reduce systematic measurement errors.

2.2. Calibration Methods and Measurement Procedures

Calibration is a fundamental step to ensure accurate S-parameter measurements. Common calibration methods include SOLT (Short-Open-Load-Through), TRL (Through-Reflection-Line), and ECal (Electronic Calibration). SOLT calibration is widely used for coaxial interfaces but requires highly precise calibration standards. TRL calibration is more suitable for PCB testing, as it reduces the influence of test fixtures and better accommodates differential interfaces. ECal offers high automation and speed, but it is relatively expensive and less flexible for custom PCB layouts. For differential high-speed PCB measurements in data center applications, TRL calibration is preferred due to its ability to isolate the device under test (DUT) from fixture-induced errors.

The measurement procedure begins with VNA warm-up to stabilize system temperature, followed by calibration using TRL standard components to construct the error model. Subsequently, the DUT is connected, the frequency range and number of data points are set according to the link specifications, and an S-parameter sweep is performed. Insertion loss (S21) and return loss (S11) data are recorded for subsequent analysis. To ensure repeatability, multiple sweeps may be conducted, and environmental conditions such as temperature and grounding are carefully controlled. This comprehensive procedure ensures that systematic and random measurement errors are minimized and that the acquired data accurately represents the intrinsic performance of the high-speed link.

2.3. Preliminary Analysis of Test Results

Initial measurements prior to de-embedding often reveal significant influence from the test fixtures. For instance, insertion loss curves may appear relatively flat at low frequencies but exhibit noticeable fluctuations at higher frequencies, indicating additional losses introduced by the fixture. Similarly, return loss curves can display prominent peaks at specific frequencies, reflecting impedance mismatches at the probe interface. These phenomena primarily stem from parasitic capacitance and inductance in the test fixtures, as well as reflection effects from connectors and cables.

In high-speed communication PCB testing, uncorrected S-parameter data is typically contaminated by systematic errors, necessitating further processing using de-embedding techniques to isolate the DUT's true characteristics. Preliminary analysis shows that fixture effects primarily manifest as frequency-dependent increases in insertion loss and degradation in return loss, which can obscure the actual signal integrity of the link. Accurate interpretation of these measurements is critical for guiding PCB design optimization, including impedance control, trace layout adjustment, and connector selection, thereby ensuring that the final high-speed link meets the stringent performance requirements of AI data center environments. Additionally, understanding the nature of these systematic errors provides insight into potential improvements in fixture design and measurement methodology, contributing to more reliable and repeatable high-frequency testing outcomes.

3. Research and Implementation of De-embedding Technology

3.1. De-embedding Principles and Mathematical Model

De-embedding techniques are essential in high-frequency testing, aiming to isolate the intrinsic electrical characteristics of a device under test (DUT) from the influence of the surrounding measurement fixtures. In practical scenarios, the fixture-comprising connectors, transmission lines, and adapters-introduces parasitic effects that can distort measured S-parameters, leading to inaccurate evaluation of the DUT. De-embedding resolves this by modeling the fixture as a two-port network that is cascaded with the DUT.

Mathematically, the DUT and the fixture are represented using either the scattering matrix (S-matrix) or the transmission matrix (T-matrix). The relationship between the S-matrix and T-matrix is defined as:

$$T = \begin{bmatrix} 1/S_{21} & -S_{22}/S_{21} \\ S_{11}/S_{21} & S_{12} - S_{11}S_{22}/S_{21} \end{bmatrix}$$

For a cascaded system, the overall T-matrix is expressed as:

$$T_{Total} = T_{fixture} * T_{DUT} * T_{fixture}$$

Hence, the DUT's T-matrix can be extracted using:

$$T_{DUT} = T_{fixture}^{-1} * T_{total} * T_{fixture*}^{-1}$$

Several de-embedding algorithms are employed in practice. Direct inversion offers computational simplicity but is highly sensitive to measurement noise, which can propagate through the matrix inversion process. Iterative optimization methods, on the other hand, are more robust against noise and modeling errors, though they require higher computational resources. The choice of algorithm depends on the trade-off between computational efficiency and measurement accuracy, particularly in high-frequency or high-speed PCB environments where even minor errors can significantly affect system performance.

3.2. Improved De-embedding Method Based on TRL Calibration

The traditional Thru-Reflect-Line (TRL) calibration technique is widely used to mitigate the impact of test fixtures, particularly by referencing measurements to known standards. However, TRL calibration alone can encounter limitations such as phase ambiguity at high frequencies, especially in complex multi-layer PCB layouts or in environments with significant temperature-induced phase drift.

To address these challenges, an improved approach integrates TRL calibration with de-embedding algorithms in a hybrid workflow. First, the fixture model is accurately characterized through TRL calibration, producing a reliable baseline for measurement corrections. Then, a de-embedding algorithm is applied to eliminate residual errors that are not fully accounted for by the calibration. Key enhancements include:

1) **Automatic phase unwrapping**: This corrects phase discontinuities and ensures the continuity of the T-matrix across frequency points.
2) **Weighted fitting of error terms**: Residual calibration errors are minimized by assigning weights according to measurement uncertainty, improving the accuracy of the extracted DUT parameters.
3) **Robust handling of environmental effects**: Temperature variations, connector repeatability, and other practical influences are considered, allowing the method to maintain accuracy in high-speed communication testing.

Such optimizations are particularly crucial for high-frequency PCB testing, where phase errors and insertion loss distortions can compromise signal integrity analyses and system design validation.

3.3. Implementation and Error Control of De-embedding Algorithm

The de-embedding algorithm is implemented in MATLAB, leveraging its matrix computation and data visualization capabilities. The workflow involves several key steps:

1) **Data import**: Original S-parameter files exported from the Vector Network Analyzer (VNA) are imported into MATLAB. File format validation and error handling are essential to prevent misinterpretation of measurement data.
2) **Fixture modeling**: Using TRL calibration results, the fixture T-matrix is calculated. Weighted fitting and optimization of residual errors ensure that the modeled fixture closely represents the real measurement environment.
3) **Matrix inversion**: The inverse of the fixture T-matrix is computed to isolate the DUT T-matrix. To mitigate numerical instability due to large condition numbers, pseudo-inverse functions (pinv) or regularization techniques are applied.

4) **S-parameter conversion**: The T-matrix of the DUT is converted back to S-parameters for analysis. The conversion process is verified against physical laws such as energy conservation to prevent unrealistic results.
5) **Results analysis**: Comparison of pre- and post-de-embedding data demonstrates the effectiveness of the method. Typically, insertion loss curves become smoother, and return loss peaks are reduced, indicating successful elimination of fixture-induced artifacts.

Error propagation in this process primarily arises from imperfect calibration, numerical errors in matrix inversion, and environmental factors affecting measurements. To control errors, the following strategies are employed:

1) **High-precision numerical algorithms**: Reducing rounding errors during matrix computations.
2) **Regularization techniques**: Stabilizing inversion of ill-conditioned matrices.
3) **Multiple averaged measurements**: Mitigating random noise and improving statistical reliability of results.

As shown in Table 1, the complete workflow, associated error sources, and control strategies are systematically organized to ensure reliable de-embedding in practical applications.

Table 1. Implementation and Error Control of the De-embedding Algorithm.

Algorithm Steps	Description	Tool	Error Source	Control Strategy
Data import	Exporting S-parameter files from VNA	MATLAB	File read error	Format validation and error handling
Fixture Modeling	Calculate the fixture T-matrix based on TRL calibration data	MATLAB functions	Calibration residual error	Weighted fitting and error term optimization
Matrix inversion	Calculate the inverse of the fixture's T-matrix	MATLAB inv ()	Numerical instability	Use pinv() or regularization
S-parameter conversion	Convert the T-matrix back to S-parameters	Custom script	Conversion error	Verify energy conservation
Results Analysis	Compare data before and after de-embedding	Drawing tools	Visual error	Statistical analysis and repeated testing

4. Discussion

The implementation and analysis of de-embedding technology in high-frequency testing provide a nuanced understanding of both its capabilities and limitations. De-embedding plays a critical role in accurately extracting the intrinsic S-parameters of the device under test (DUT) by effectively eliminating the parasitic influence of measurement fixtures. The results obtained through MATLAB-based implementation demonstrate the feasibility of combining traditional calibration methods with advanced algorithmic processing to achieve high-fidelity DUT characterization.

One of the main advantages of the described de-embedding methods is the ability to correct for systematic errors introduced by the measurement setup. By modeling the fixture as a two-port network and employing either direct inversion or iterative optimization, the approach ensures that the measured responses reflect the DUT itself rather than the cascade effects of connectors, transmission lines, and adapters. The integration of TRL calibration with a subsequent de-embedding procedure further enhances accuracy by accounting for residual errors that cannot be eliminated by

calibration alone. In particular, automatic phase unwrapping and weighted error fitting are effective in addressing phase discontinuities and calibration imperfections, which are common challenges in high-speed PCB testing and millimeter-wave frequency applications.

Despite these advantages, several limitations warrant careful consideration. Direct inversion, while computationally simple, is sensitive to noise and measurement uncertainty. Even minor errors in the fixture model can propagate through the inversion process, potentially leading to unrealistic DUT S-parameters. Iterative optimization techniques mitigate this issue but at the cost of increased computational complexity, which may become significant when handling large datasets or multi-port networks. Moreover, environmental factors such as temperature fluctuations, connector repeatability, and vibration can introduce additional uncertainty that requires careful averaging and statistical treatment.

Error analysis and control are therefore central to the practical application of de-embedding techniques. The use of high-precision numerical algorithms and matrix regularization methods reduces the risk of instability during matrix inversion. Multiple averaged measurements help to counteract random noise and provide more reliable parameter estimates. Additionally, validation of S-parameter conversions against physical laws such as energy conservation ensures that the extracted data remain physically meaningful. These strategies collectively contribute to the robustness of the de-embedding process in realistic testing conditions.

From a broader perspective, the implementation of de-embedding technology has significant implications for the design, optimization, and validation of high-speed communication systems. Accurate extraction of DUT characteristics allows engineers to better assess signal integrity, evaluate crosstalk, and design PCB layouts with minimized insertion loss and reflection. This capability is particularly critical in emerging applications such as 5G, millimeter-wave radar systems, and high-speed serial communication interfaces, where even small deviations in S-parameters can adversely affect overall system performance.

Looking forward, there are several avenues for further improvement. Integration of machine learning techniques to predict and compensate for systematic errors could further enhance the accuracy and efficiency of de-embedding. Adaptive algorithms that automatically select the optimal calibration and de-embedding method based on measurement conditions could also reduce manual intervention and improve repeatability. Additionally, extending the de-embedding framework to multi-port, multi-layer PCB networks and complex heterogeneous fixtures remains an important challenge, as does the need for real-time de-embedding in automated test environments.

In conclusion, while de-embedding technology presents certain computational and practical challenges, its ability to isolate true DUT characteristics from measurement artifacts makes it indispensable for precise high-frequency testing. The combination of TRL calibration, robust de-embedding algorithms, and rigorous error control not only enhances measurement accuracy but also enables engineers to better understand and optimize high-speed electronic systems. Continuous methodological improvements and integration with emerging computational techniques promise to further expand the utility and applicability of de-embedding in both research and industrial contexts.

5. Conclusion

This study presents a comprehensive investigation of insertion loss and return loss measurements for high-speed serial links on printed circuit boards (PCBs), with particular focus on the implementation and refinement of de-embedding techniques using a Vector Network Analyzer (VNA). In the context of rapidly evolving high-speed communication systems, such as those deployed in artificial intelligence data centers and advanced computing environments, precise characterization of signal integrity is critical for

ensuring reliable data transmission and optimal system performance. The research addresses this demand by analyzing the underlying principles of VNA measurements, identifying the specific testing requirements for high-speed PCB links, and proposing a robust test system design capable of accommodating complex practical scenarios.

A central contribution of this work is the development of an enhanced de-embedding methodology that effectively isolates the intrinsic electrical properties of the device under test (DUT) from the parasitic effects introduced by measurement fixtures, including connectors, adapters, and transmission lines. Traditional calibration methods, while useful, are often insufficient to completely remove residual errors, particularly at high frequencies where phase ambiguities and fixture-induced distortions become pronounced. By integrating Thru-Reflect-Line (TRL) calibration with advanced de-embedding algorithms, including automatic phase unwrapping and weighted error term optimization, the proposed approach demonstrates superior accuracy in capturing the true S-parameters of the DUT. Experimental results show that this method successfully smooths insertion loss curves and reduces return loss peaks, indicating a significant mitigation of fixture-induced measurement errors.

The study also emphasizes practical implementation aspects, including the use of MATLAB for data processing, fixture modeling, matrix inversion, and S-parameter conversion. By adopting high-precision numerical techniques, regularization methods, and multiple averaged measurements, the approach addresses common sources of error such as numerical instability, random noise, and calibration imperfections. These strategies collectively enhance the reliability and reproducibility of the measurements, ensuring that the extracted DUT characteristics accurately reflect the real-world performance of high-speed PCB links.

Beyond the immediate technical contributions, the findings of this study provide meaningful guidance for industry practitioners involved in the design, testing, and validation of high-speed communication systems. Accurate measurement of insertion loss and return loss, coupled with robust de-embedding, enables engineers to make informed decisions regarding PCB layout optimization, signal integrity analysis, and overall system design. This is particularly crucial in scenarios where even minor deviations in S-parameters can lead to signal degradation, increased error rates, or reduced system reliability. By offering a practical and validated methodology, the research supports improved performance assessment and design verification in cutting-edge electronic systems.

Finally, the results of this study highlight the broader implications of integrating advanced measurement and de-embedding techniques in high-speed electronics testing. The proposed framework not only enhances measurement accuracy but also provides a scalable and adaptable solution that can be extended to multi-port, multi-layer PCB networks and other complex electronic configurations. Future work may focus on incorporating real-time automated de-embedding, adaptive calibration procedures, and computational intelligence techniques to further enhance the efficiency and robustness of the testing process. Overall, this study establishes a solid foundation for the precise evaluation of high-speed PCB links, contributing to the development of reliable, high-performance communication systems and offering actionable insights for both research and industrial applications.

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